REMARKS

In the Office Action of August 4, 2006, the Examiner (1) rejected claims 1-3, 6 and 19-20 under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,041,399 ("*Terada*"); 2) rejected claims 4-5 and 7-9 under 35 U.S.C. § 103 as being unpatentable over *Terada* in view of U.S. Patent No. 5,659,722 ("*Blaner*"); 3) rejected claim 10 under 35 U.S.C. § 103 as being unpatentable over *Terada* in view of *Blaner* and U.S. Patent No. 5,504,903 ("*Chen*"); 4) rejected claims 11-13, 16 and 18 under 35 U.S.C. § 103 as being unpatentable over *Terada* in view of U.S. Patent No. 6,088,786 ("*Freierbach*"); and 5) rejected claims 14-15 and 17 under 35 U.S.C. § 103 as being unpatentable over *Terada* in view of *Blaner* and *Freierbach*.

In this Response, Applicants amend claims 1 and 19. Based on the amendments and arguments presented herein, Applicants respectfully request reconsideration and allowance of the pending claims.

CLAIM REJECTIONS

Claims 1-3, 6 and 19-20 were rejected under 35 U.S.C. § 102 as being anticipated by *Terada*. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claim 1 has been amended to recite a "processor [that] executes a routine having a test and skip instruction that includes an immediate value and a reference to a register, the test and skip instruction performs a comparison using the immediate value and the register value stored in the referenced register, and selectively skips a subsequent instruction that follows the test and skip instruction based on the comparison". Claim 1 further requires that "the subsequent instruction jumps to another routine".

Regarding claim 1, *Terada* fails to teach Applicants' claimed "test and skip instruction" where "the subsequent instruction jumps to another routine". Instead,

Terada simply shows various examples of selectively skipping instructions for subtraction, addition, multiplication, and division (see Figures 4, 8, 9, 11, 12, 15). For at least this reason, claim 1 and its dependent claims are allowable over *Terada*.

Claim 19 has been amended to recite "means for selectively changing an operating mode of the programmable logic device". Claim 19 further recites "means for decoding an instruction that includes an immediate value and a reference to a register for performing a comparison using the immediate value and a register value stored in the referenced register, and for causing the processor to execute or not execute a subsequent instruction that follows the instruction based on the comparison." Claim 19 further recites "the subsequent instruction jumps to a routine associated with a particular operating mode."

Regarding claim 19, *Terada* fails to teach Applicants' claimed "means for selectively changing an operating mode of the programmable logic device". Furthermore, Terada fails to teach Applicants' claimed instruction which compares an immediate value with a register value and selectively executes "a subsequent instruction" based on the comparison, where the "the subsequent instruction jumps to a routine associated with a particular operating mode." Instead, *Terada* shows various examples of selectively skipping instructions for subtraction, addition, multiplication, and division without mentioning different operating modes. For at least these reasons, claim 19 and its dependent claim are allowable over *Terada*.

Claims 4-5 and 7-9 were rejected under 35 U.S.C. § 103 as being unpatentable over *Terada* in view of *Blaner*.

Regarding claim 9, Applicants respectfully disagree with the Examiner's assertions because the Examiner has failed to establish a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion of motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art must teach or suggest all the claim limitations" (MPEP

2143). "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Regarding claim 9, the Examiner recognizes that the cited references fail to teach or suggest all the claim limitations as is required (see Office Action 08/04/06, page 13, last full paragraph). Specifically, the first and second states of Applicants' claimed "control bit" are not taught by the cited references. Thus, the Examiner has failed to provide objective evidence for rejecting claim 9. For at least this reason, claim 9 and its dependent claims are allowable over the cited references.

Claims 11-13, 16 and 18 were rejected under 35 U.S.C. § 103 as being unpatentable over *Terada* in view of *Feierbach*.

Regarding claim 11, Applicants respectfully disagree with the Examiner's assertions because the Examiner has failed to establish a *prima facie* case of obviousness. *Feierbach* fails to teach "a co-processor [which] selectively operates in a stack-based instruction mode and a register-based instruction mode" as set forth in claim 11. Instead, *Feierbach* shows a stack processor 202 which is separate from a register processor 204 (see Figure 2). None of the references cited by the Examiner, considered individually or together, teach or suggest Applicants' claimed co-processor. For at least this reason, claim 11 and its dependent claims are allowable over the cited references.

CONCLUSIONS

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. Applicants hereby petition for any time extensions that are necessary to prevent this case from being abandoned. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims and for time extension), the Examiner is authorized to charge Texas Instruments Inc.'s Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

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